

UNITED STATES PATENT APPLICATION FOR

CIRCUIT AND SYSTEM FOR ADDRESSING MEMORY MODULES

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CIRCUIT AND SYSTEM FOR ADDRESSING MEMORY MODULES TECHNICAL FIELD

The present invention relates to the field of computer systems. Specifically, embodiments of the present invention relate to a circuit and system for addressing
5 multiple computer memory modules on the same bus while maintaining proper timing.

BACKGROUND ART

Figure 1 illustrates a conventional circuit 100 for addressing several memory modules 110. For example, the configuration of Figure 1 may be used for double data
10 rate (DDR) synchronous dynamic random access memory (SDRAM). Typically, the configuration consists of two to four dual inline memory modules (DIMM) that are connected together by daisy chaining the modules together as shown in Figure 1.

Resistors are used to avoid problematic reflections and to properly terminate
15 the address signal. A series resistor 120 between the driver 125 and the memory modules 110 serves to dampen reflected signals coming back from the memory modules 110. The parallel resistor 130 coupled to the terminating voltage 140 serves to properly terminate the signal and typically has an impedance to match that of the transmission line 150.

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Such a conventional system functions well when the number of memory modules 110 is limited to no more than four memory modules 110. However, the need for ever more memory has led to a desire to place more than four memory modules together in a fashion such that they can all be addresses by a single driver.

Unfortunately, if more than four modules are daisy chained in the configuration of Figure 1, the distance between the memory modules 110 leads to unacceptable skew. That is, it takes too long for the address signal to travel from the first to the fifth or more memory module, given the timing budget.

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One conventional technique to increase the number of memory modules in the overall system is to add an additional driver to the system such that a few more memory modules can be addressed within the timing budget. However, this solution is undesirable because the additional driver requires additional space, which is limited in many computer systems.

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Thus, one problem with conventional methods of addressing memory in a computer system is that timing skew limits how many memory modules can be addressed using a single driver. Another problem with conventional techniques is that too much space is required by the number of drivers that are required to address the desired number of memory modules.

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DISCLOSURE OF THE INVENTION

The present invention pertains to a circuit and system for a heavily loaded memory module address bus. In one embodiment, the circuit comprises a transmission line having a dampening impedance between a driver and a branch point of the
5 transmission line. The circuit also has a termination impedance having one end coupled to the transmission line between the dampening impedance and the branch point. The transmission line has branches from the branch point. Each branch couples to at least one memory module interface.

BRIEF DESCRIPTION OF THE DRAWINGS

The accompanying drawings, which are incorporated in and form a part of this specification, illustrate embodiments of the invention and, together with the description, serve to explain the principles of the invention:

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Figure 1 illustrates a conventional configuration for addressing memory modules.

Figure 2 is a diagram of a circuit for addressing multiple computer memory
10 modules on the same bus while maintaining proper timing, according to embodiments of the present invention.

Figure 3A is a diagram of a location for impedances for addressing multiple computer memory modules on the same bus while maintaining proper timing,
15 according to embodiments of the present invention.

Figure 3B is a diagram of an alternative location for impedances for addressing multiple computer memory modules on the same bus while maintaining proper timing, according to embodiments of the present invention.

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Figure 4 is a side view of a system for addressing multiple computer memory modules on the same bus while maintaining proper timing, according to an embodiment of the present invention.

DETAILED DESCRIPTION OF THE INVENTION

In the following detailed description of embodiments of the present invention, a circuit and system for addressing multiple computer memory modules on the same bus while maintaining proper timing, numerous specific details are set forth in order to provide a thorough understanding of the present invention. However, embodiments of the present invention may be practiced without these specific details or by using alternative elements or methods. In other instances well known methods, procedures, components, and circuits have not been described in detail as not to unnecessarily obscure aspects of the present invention.

Embodiments of the present invention reduce skew when addressing multiple computer memory modules on the same bus while maintaining proper timing, as compared to conventional solutions. Embodiments of the present invention use a single driver to address more than four memory modules. Embodiments of the present invention allow termination resistors to be placed relatively far from the memory modules being addressed. Thus, embodiments of the present invention provide more freedom in selecting the location of termination resistors.

Figure 2 is a circuit 200 for accessing memory modules 340, according to an embodiment of the present invention. The circuit 200 allows the number of memory modules that are addressed to be doubled, as compared to the conventional circuit in Figure 1, without an increase in the timing skew. Moreover, the configuration of

dampening and termination impedances allows for signal transmission with adequate signal integrity to address the memory modules 340.

The circuit 200 has a transmission line 320 that is coupled at one end to a
5 driver 305 and coupled to interfaces 330 that are able to receive memory modules 340. The transmission line 320 is uni-directional in embodiments of the present invention. The transmission line 320 has a branch point 315 from which two branches 320c, 320d of the transmission line extend. A first branch 320c extends from the branch point 315 to memory module connector 340a. A second branch 320d extends from the
10 branch point 315 to memory module connector 340i. The first branch 320c electrically connects to memory module connectors 340a, 340b, 340c, and 340d. The second branch 320d electrically connects to memory module connectors 340e, 340f, 340g, and 340h. Thus, each branch 320c and 320d is used to address four memory modules, such that a single driver 305 is used to address eight memory modules 340. Thus, the
15 number of memory modules 340 that can be addressed by a single driver 305 is doubled over the conventional circuit of Figure 1, while still maintaining proper timing. The two branches 320c, 320d of the transmission line are also referred to herein as an address line. Embodiments of the present invention are not limited to the transmission line having only two branches.

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Still referring to Figure 2, the transmission line 320 comprises a series dampening impedance 350. The dampening impedance 350 is between a segment of the transmission line 320a coupled to the driver 305 and a segment of the transmission

line 320b between the dampening impedance 350 and the branch point 315. The circuit 300 also has a parallel termination impedance 360 having one end coupled to a node 365 on the transmission line 320 between the dampening impedance 350 and the branch point 315. The termination impedance 360 is connected to the dampening
5 impedance 350, in one embodiment of the present invention. However, it is not required that the dampening impedance 350 and the termination impedance 360 be connected without any intervening element. The other end of the termination impedance 360 is coupled to a termination voltage 370.

10 Referring briefly to Figure 1, the purpose of the pull-up parallel termination resistor 130 is to terminate the signal at the end of the transmission line 115. As such, it is not considered intuitive to place a parallel termination resistor on the same side of the memory modules as the driver. Referring now to Figure 2, the termination
impedance 360 is placed on the same side of the memory modules 340 as the driver
15 305. As positioned, the combination of the series dampening impedance 350 and the parallel termination impedance 360 prevents, or at least reduces, reflections from the memory modules 340 from travelling back to the driver 305 in the region of the transmission line 320a between the parallel termination resistor 360 and the driver
305. There may be some reflections in the region of the transmission line 320b
20 between the parallel termination resistor 360 and the branch point 315, as well as on the branches of the transmission line 320c and 320d.

However, embodiments of the present invention are configured such that reflections between the parallel termination resistor 360 and the memory modules 340 do not cause significant signal integrity problems. For example, the memory modules 340 are located very close to each other relative to the size of the wavelength of a
5 typical signal.

The transmission line 320 branches at branch point to achieve a symmetrical configuration in the various branches of the data line 320, in embodiments in accordance with the present invention. Thus, not only is skew reduced when
10 addressing the memory modules, but the symmetry reduces the complexity in analyzing the system during design and test phases.

In the conventional circuit of Figure 1, the resistors 120, 130 should be near the memory modules 110. However, with some system designs it is not practical or
15 even possible to locate the dampening and termination impedances near the memory modules. Embodiments of the present invention allow the dampening and termination impedances to be a long distance from the memory modules. In one embodiment of the present invention the distance from point 365 at which the termination impedance 360 connects to the transmission line 320 to the branch point 315 is greater than the
20 length of the branches of the transmission line 320c, 320d.

Moreover, in embodiments of the present invention, the configuration of the series dampening impedance 350 and the parallel termination impedance 360 provides

flexibility in controlling the magnitude of the signal on the transmission line 320 not available in the conventional circuit of Figure 1. The series dampening impedance 350 and the parallel termination impedance 360 form a voltage divider. By selecting appropriate impedance values for the series dampening impedance 350 and the
5 parallel termination impedance 360, the magnitude of the signal on the transmission line 320 is controlled, according to an embodiment of the present invention.

For clarity, Figure 2 only depicts a single set of components. Embodiments of the present invention have numerous sets of components each for delivering address
10 data to separate pins of respective memory module interfaces 330.

There may be more or fewer memory module connectors 330 than shown in Figure 2. Moreover, it is not required that all of the memory module connectors 330 contain memory modules 340.

15 Moreover, the dampening and termination impedances can be located on the side of the memory module connectors rather than on the end of the memory modules. For example, referring to the conventional circuit of Figure 1, the series dampening resistor 120 is adjacent to one end of the chain of memory modules 110 and the
20 parallel termination resistor 130 is at the other end of the chain of memory modules 110. Referring to Figure 3A, the series dampening impedance 350 and the parallel termination impedance 360 are located adjacent to the side of the chain of memory modules 340.

In Figure 3A, the series dampening impedance 350 and the parallel termination impedance 360 are near the middle of the chain of memory modules 340. However, the impedances can be located anywhere along the edge from the first to last memory module 340. In Figure 3B, the series dampening impedance 350 and the parallel termination impedance 360 are located adjacent to the side of the chain of memory modules 340 at a spot between the first and second memory modules 340 in the chain. As it is not required that the dampening impedance 350 and the parallel termination impedance 360 be located close to the branch point 315, embodiments of the present invention provide greater freedom in locating the impedances than does the convention circuit of Figure 1. Thus, the embodiments of Figures 3A and 3B are exemplary of many possible locations for the series dampening impedance 350 and the parallel termination impedance 360.

In embodiments of the present invention, the waveform that is transmitted on the transmission line 320 is a square wave that is used as a data signal. That is, the rising or falling edges of the waveform are not used for clocking purposes. Therefore, the rising and falling edges of the waveform are not critical. However, the top and bottom of the waveform are significant for the data value to be registered properly. Even if there is some deformity in the edges of the waveform, the data value will still be interpreted properly if the tops and bottoms of the waveform do not experience significant distortion. For example, the data value will still be interpreted properly if the tops and bottoms of the waveform are within specification for the memory

modules 340 in the circuit 300. The present invention provides for such a waveform in which the tops and bottoms of the waveform have a distortion that is small enough so as to not cause improper values to be registered.

5 Figure 4 is a side view of a system 500 for accessing memory modules, according to an embodiment of the present invention. Figure 4 illustrates one possible placement for the dampening and termination impedances with respect to a printed circuit board. The system 500 includes a printed circuit board (PC board) 510 upon which the dampening and termination impedances 350, 360 are mounted on opposite
10 sides. Also mounted on the PC board 510 are a controller 515 and memory module connectors 340.

 The dampening and termination impedances 350, 360 are electrically coupled by a line through the via 545 in the PC board 510. Placing the dampening and
15 termination impedances 350, 360 on opposite sides of the PC board 510 may allow for a more compact PC board 510 than if both impedances 350, 360 are placed on the same side of the PC board 510, although it is not required that the impedances be located on opposite sides of the PC board 510.

20 The system 500 includes a transmission line 320 that couples the controller 515 with the memory module connectors 340. A portion of the transmission line 320a is coupled between the controller 515 and the dampening impedance 350. The dampening impedance 350 may also be referred to as a series impedance. Another

portion of the transmission line 550b is coupled between the dampening impedance 350 and the memory module connectors 340. This portion of the transmission line 550b run partway through the via 545. A first end of the termination impedance 360 is electrically coupled to the transmission line 550 by termination impedance line 555.

- 5 A second end of the termination impedance 360 is electrically connected to a termination voltage terminal 570.

The second portion of the transmission line 550 couples to a branch point 315 of the transmission line 320, which branches into two separate parts 320c and 320d.

- 10 Each branch 320c, 320d of the transmission line couples to four memory module connectors 340, in this embodiment. However, the present invention is not limited to a branch being connected to four memory module connectors. Moreover, the present invention is not limited to only two branches. The embodiment of Figure 4 allows the controller 515 to comprise a single driver that addresses eight memory modules while
- 15 staying within the timing budget. The memory modules are not depicted in Figure 4. In one embodiment in accordance with the invention, the memory modules are dual inline memory modules (DIMMs). The memory itself is double data rate (DDR) synchronous dynamic random access memory (SDRAM), in accordance with an embodiment of the present invention.

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While the present invention has been described in particular embodiments, it should be appreciated that the present invention should not be construed as limited by such embodiments, but rather construed according to the below claims.